

-2-

ONS00470  
10/773,853Amendments to the Claims

1. (currently amended): A method for forming an isolation ~~tub~~ region comprising the steps of:  
providing a region of semiconductor material;  
forming a tub in the region of semiconductor material,  
wherein the tub includes a plurality of shapes in the region of  
semiconductor material; and  
exposing the plurality of shapes to an ambient that includes a chemical species that reacts with the plurality shapes to form the low capacitance isolation region, and wherein the plurality of shapes form part of the isolation region. tub.
2. (currently amended): The method of claim 1 wherein the step of exposing includes thermally oxidizing the plurality of shapes to form a silicon oxide isolation region. tub.
3. (currently amended): The method of claim 1 ~~further comprising the step of~~ wherein the step of forming the tub includes forming the tub having a boundary around the plurality of shapes, wherein the boundary includes a recessed portion.
4. (original): The method of claim 1 wherein the step of exposing includes consuming substantially all of the plurality of shapes.
5. (currently amended): The method of claim 1 further comprising the step of forming a passive device over the ~~low capacitance isolation region. tub.~~
6. (currently amended): The method of claim 1 wherein the step of forming the tub ~~plurality of shapes~~ includes etching exposed portions of the region of semiconductor material, and wherein the plurality of shapes comprise unexposed portions of the region of semiconductor material.

-2-

-3-

ONS00470  
10/773,853

7. (original): The method of claim 6 wherein the step of etching includes etching to a depth from about 6 microns to about 10 microns.

8. (currently amended): The method of claim 1, wherein the step of forming the tub ~~plurality of shapes~~ includes forming a tub having a matrix of free standing shapes, wherein adjacent rows of shapes are offset from each other.

9. (original): The method of claim 1 wherein the step of providing the region of semiconductor material includes providing a region comprising silicon.

10. (currently amended): A process for forming an integrated circuit device including the steps of:

forming a tub region ~~a matrix of shapes~~ within a semiconductor layer, wherein tub region includes a ~~the~~ matrix of shapes comprising ~~comprises~~ offset rows; and  
forming a dielectric region within the matrix of shapes.

11. (currently amended): The process of claim 10 wherein the step of forming the tub region includes forming a tub region with a matrix of ~~shapes~~ ~~includes forming a matrix of~~ squares.

12. (original): The process of claim 10 wherein the step of forming the dielectric region includes oxidizing the matrix of shapes.

13. (original): The process of claim 12 wherein the step of oxidizing forms a nearly continuous silicon oxide tub.

14. (original): The process of claim 10 further comprising the step of forming a passive component over the dielectric region.

-3-

-4-

ONS00470  
10/773,853

15. (original): The process of claim 10 further comprising the step of forming an isolation trench in the region of semiconductor material.

16. (original): The process of claim 10 further comprising the steps of:

forming a dielectric layer on sidewalls of the matrix of shapes; and

forming a polycrystalline semiconductor layer over the dielectric layer.

17. (currently amended): The process of claim 10 wherein the step of forming tub region ~~the matrix of shapes~~ includes forming tub region having a matrix of shapes wherein shapes in a first row have a first spacing, and wherein the shapes in the first row have a second spacing from shapes in a second row, and wherein the second spacing is less than the first spacing.

18. (currently amended): A semiconductor device comprising:  
a region of semiconductor material; and  
a dielectric tub formed in the region of semiconductor material, wherein the dielectric tub includes ~~comprising~~ a matrix of passivated shapes, and wherein adjacent rows of passivated shapes are offset.

19. (original): The device of claim 18 wherein the dielectric tub comprises oxidized silicon shapes.

20. (original): The device of claim 18 wherein the dielectric tub includes a boundary having a recessed portion.

-4-